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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,680	12/16/2003	Takahito Nakano	246575US6	3581
22850	7590	04/16/2007	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			FRANKLIN, RICHARD B	
		ART UNIT		PAPER NUMBER
				2181
SHORTENED STATUTORY PERIOD OF RESPONSE		NOTIFICATION DATE	DELIVERY MODE	
3 MONTHS		04/16/2007	ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/16/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)
	10/735,680	NAKANO ET AL.
	Examiner	Art Unit
	Richard Franklin	2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 29 January 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,4,5 and 7-9 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,4,5 and 7-9 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1, 4 – 5, and 7 – 9 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 4 – 5, and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
3. Claim 1 recites the limitation "control means" in line 14 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the "connection control means" first recited in line 10 or a new "control means."

The Examiner has interpreted the limitation to refer to a new control means.

4. Regarding claim 5, the word "means" is preceded by the word(s) "storage" in an attempt to use a "means" clause to recite a claim element as a means for performing a specified function. However, since no function is specified by the word(s) preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967).

5. Claim 5 recites the limitation "the storage means" in lines 10, 11, 15, and 16 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the "storage means" first recited in line 3 or the "semiconductor information storage means" first recited in line 4.

The Examiner has interpreted the limitation to refer to the "storage means" of line 3.

6. Claim 8 recites the limitation "control means" in line 14 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the "connection control means" first recited in line 10 or a new "control means."

The Examiner has interpreted the limitation to refer to a new control means.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,794,066 (hereinafter Dreyer).

As per claims 1 and 8, Dreyer teaches a semiconductor integrated circuit apparatus (Figure 1 Item 10) comprising a semiconductor information storage means

(Figure 1 Item 30, Col 5 Lines 11 – 16) for storing semiconductor information unique to the semiconductor integrated circuit apparatus, and semiconductor information output means (Figure 1 Item 40) connected to the semiconductor information storage means for reading out the semiconductor information from the semiconductor information storage means in response to an externally supplied signal (Col 6 Lines 6 – 11), and outputting the read-out semiconductor information (Col 6 Lines 6 – 11, Col 6 Lines 44 – 50), wherein the semiconductor information output means includes connection control means (Figure 1 Item 41), which is configured to be connected to external storage means storing an executable program (Figure 1 Item 12), for controlling a read-out operation of the program stored in the external storage means (Col 6 Lines 6 – 8, Col 6 Lines 32 – 38), the program being used for executing the read-out operation of the semiconductor information (Figure 1 Item 54, Col 6 Lines 32 – 38), and control means (Figure 1 Item 42) for controlling the read-out operation and external outputting operation of the semiconductor information by executing the read-out program read by the connection control means (Col 6 Lines 45 – 51).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,794,066 (hereinafter Dreyer) in view of the Examiners taking of Official Notice.

As per claim 4, Dreyer teaches the semiconductor integrated circuit apparatus as described per claim 1 (see rejection of claim 1 above). Dreyer also teaches wherein the semiconductor information storage means stores an identification code as the semiconductor information (Figure 1 Item 30), the identification code being assigned to allow identification of the semiconductor integrated circuit apparatus (Col 4 Lines 30 – 33). Dreyer also teaches wherein the semiconductor information storage means outputs an electric signal according to the identification code in response to an input of a signal.

Dreyer does not explicitly teach outputting the data in response to a signal.

However, the Examiner takes Official Notice that it is well known in the art of data storage to provide a read signal to a memory in order to read its contents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Dreyer to include the data output signal because doing so allows for the memory to know when to output the data.

9. Claims 5, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,794,066 (hereinafter Dreyer) in view of US Patent No. 6,065,113 (hereinafter Shiell).

As per claims 5 and 7, Dreyer teaches a circuit board on which a semiconductor integrated circuit apparatus comprising a storage means (Dreyer; Figure 1 Item 12), semiconductor information storage means (Dreyer; Figure 1 Item 30) for storing semiconductor information unique to the semiconductor information circuit apparatus, and semiconductor information output means (Dreyer; Figure 1 Item 40), which is configured to be connected to the semiconductor information storage means, for reading out the semiconductor information from the semiconductor information storage means in response to a signal supplied from outside (Dreyer; Col 6 Lines 6 – 11, Col 6 Lines 32 – 38) and wherein the storage means stores an executable program being used for executing the read-out operation of the semiconductor information (Dreyer; Figure 1 Item 54), and wherein the semiconductor information output means controls the read-out operation of the semiconductor information by executing the program read out from the storage means (Dreyer; Col 6 Lines 32 – 38). Dreyer also teaches writing the semiconductor information into a storage means (Dreyer; Figure 1 Items 20 or 22, Col 6 Lines 32 – 38).

Dreyer does not teach writing the semiconductor information to the storage means storing the read-out program.

However, Shiell teaches outputting the semiconductor information identifier code from the device so that it may be used by an application program (Shiell; Figure 1 Item 18, Col 3 Lines 36 – 39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Dreyer to include the

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external outputting because doing so allows for use by features such as the BIOS, an operating system, or an application program (Shiell; Col 3 Lines 36 – 39).

As per claim 9, Shiell also teaches wherein the semiconductor information includes at least one of a wafer number, information of a position on a wafer, and a manufacture time of the semiconductor integrated circuit (Shiell; Figure 2).

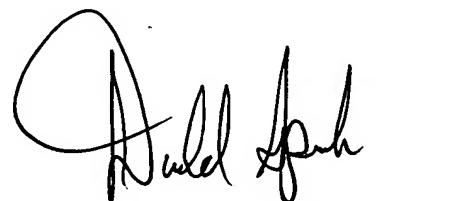
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
Patent Examiner
AU 2181



DONALD SPARKS
SUPERVISORY PATENT EXAMINER